

Design of SSB Communication System based on Carrier Synchronization Extraction

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Abstract: A novel design and implementation method of all digital phase-locked loop (DPLL) for carrier synchronization of digital coherent demodulation in SSB Direct-sequence spread spectrum communication system is proposed. The full digital phase-locked loop Phase detector and numerical controlled oscillator are implemented in vector mode and rotation mode of the algorithm respectively, and an appropriate compromise is made between the number of iterations and the complexity of the algorithm. According to the characteristics of the proposed multi-step correlation algorithm, the distribution pattern of pilot frequency and data composition is optimized. The simulation results show that, taking a system where 6 users share 4 resource blocks as an example, the carrier synchronization scheme based on optimized frame structure can achieve higher estimation accuracy and better bit error performance with less pilot overhead compared to using classical frame structure.

Keywords: SSB communication, carrier synchronization, synchronization extraction

1. INTRODUCTION

In recent years, with the rapid development of new application scenarios such as the Internet of Things and machine communication, ground networks have shown certain limitations in terms of construction cost, maintenance cost, coverage range, etc. . Therefore, at the conference 3GPP RAN, solutions for non-terrestrial networks have been incorporated into the fifth generation (5G) mobile communication standard, aiming to compensate for the shortcomings of terrestrial networks in signal coverage, service quality, and other aspects .

Among them, as an important part of the non-ground network, LEO satellite communication has the advantages of low Transmission delay, low link loss, high system reliability, etc. , which can quickly achieve a wide range of coverage. Sync and go, which means fast data transfer between devices, such as downloading high-definition (HD) movies from a self-service station (kiosk) to a handheld terminal, or quickly exchanging photos between smartphones.

Communication speed is the primary consideration for this application, especially when it comes to transferring large files. The transmission distance of this application generally does not exceed 1 meter, so the channel mode is generally dominated by LOS. The main idea of NOMA technology is to provide services to multiple users on the same resource block, using complex detection algorithm design and interference cancellation technology at the receiving end to separate user information. Compared with orthogonal multiple access (OMA), the SCMA indicator matrix is shown in equation. The receiver uses the MPA algorithm for multiuser detection. Table 1 shows the frequency offset and phase offset sizes set on each resource block. The range of the ratio E_b/N_0 of the average energy of each simulation bit to the Spectral density of the noise unilateral power can be roughly determined by using the error probability theoretical derivation and simulation results in reference and combining with the actual situation, which is set at 14-20dB.

NOMA technology can significantly improve resource utilization and system throughput and has a competitive advantage in communication scenarios with massive user

access (such as satellite IoT). The existing NOMA schemes can be roughly divided into two categories: power domain-based NOMA technology and code domain-based NOMA technology. Among them, the former distinguishes different users through power allocation , but it is difficult to achieve in satellite communication with limited power. The latter uses specific structures or mappings to distinguish different users, and is less affected by power, making it more suitable for low orbit satellite communication.

Sparse code multiple access (SCMA) technology is a typical non orthogonal multiple access technology based on the code domain . By distinguishing different users through different sparse codebooks, it can achieve high overload rates while maintaining good performance, thus gaining widespread attention. In addition, its flexible codebook design provides rich optimization dimensions, making it more suitable for low orbit satellite communication systems. Although the complex multiuser detection algorithm still has certain limitations in the practical application of SCMA technology

2. THE PROPOSED METHODOLOGY

2.1 Design of Communication System Based on Carrier Synchronization Extraction

This article will study the related issues of SCMA technology in satellite communication systems. The most direct method for carrier synchronization is the insertion pilot method. From a time, domain perspective, it means sending one or more sine waves as pilot signals in addition to useful signals. From a frequency domain perspective, it means adding spectral lines at appropriate spectral positions, and the receiver uses a filter to extract this spectral line separately to obtain carrier frequency information, so this method is also known as external synchronization method. The system error rate curve after adding carrier frequency offset and performing carrier synchronization basically coincides with the system error rate curve without frequency offset, that is, the impact of carrier frequency offset on the simulation system is basically eliminated. After comprehensively referring to the schematic diagram of the impact of carrier frequency offset on the system error rate, a conclusion can be drawn, the carrier

synchronization algorithm described in this chapter can effectively correct the carrier frequency offset in both LOS and NLOS channels, and the algorithm design has achieved the expected results.

In low orbit satellite communication, a large Doppler frequency shift can cause frequency and phase shifts in the received signal, leading to a sharp decline in receiver performance. Currently, a carrier synchronization module is required to capture and track the two. In the carrier synchronization module, a stepwise correlation frequency offset estimation algorithm and a maximum likelihood phase offset estimation algorithm are designed using the unmodulated pilot signal.

This chapter first provides an overview of traditional carrier synchronization algorithms, detailing the Costas loop carrier synchronization algorithm and the data-assisted carrier synchronization algorithm. Then, the data-assisted carrier synchronization algorithm leads to the carrier synchronization algorithm based on gray sequence correlation operation, and the two-step carrier synchronization process is detailed in conjunction with the frame structure. Finally, simulation testing was conducted, and the conclusion was drawn that the algorithm meets the project design requirements. Finally, this chapter introduces the low hardware complexity processing details of the synchronization algorithm. When pilot overhead $\eta < 20\%$, the carrier synchronization scheme, especially the frequency offset estimation algorithm, has a significant estimation error, which leads to serious degradation of system performance. When pilot overhead $\eta = 20\%$, the overall estimation accuracy of the carrier synchronization scheme is relatively high, thus achieving a near ideal situation. The BER performance of $\text{fITs}=0$, with $\text{BER}=10^{-4}$ as an example, corresponds to a performance loss of approximately 0.3dB.

LOS channel, signal-to-noise ratio 8dB). Note that the sampling deviation in the table is not the sampling frequency deviation, but the sampling point position deviation. From the diagonal data, when the sampling bias of the preamble and subsequent data blocks of the frame is consistent, the fractional equalizer of this system can effectively correct the impact of sampling timing deviation. The system error rate is basically maintained at 45, but there are significant fluctuations in the error rate in other positions in the table, corresponding to changes in the actual sampling bias. At this time, the equalizer fails to correct the impact caused by sampling timing deviation.

2.2 Application of Carrier Synchronization in SSB Communication System

There is no need to adjust the ADC sampling clock, which avoids the problem of unsatisfactory correction of sampling timing deviation caused by clock adjustment lag in high-speed communication systems. The digital timing synchronization system performs ADC sampling at a fixed local sampling frequency and phase, with a sampling rate typically several times the symbol rate. This allows for the recovery of an optimal sampling point using multiple sample points. Considering the characteristics of the baseband gigabit processing rate of this project, the traditional feedback adjustment method for ADC sampling clock is no longer applicable. Therefore, this article mainly analyzes the digital timing synchronization method.

To demonstrate the advantages of optimizing frame structure, pilot overhead is provided $\eta = 15\%$ and $\eta = 20\%$, the BER performance of carrier synchronization schemes based on

optimized structure-1 and optimized structure-2 is compared with corresponding classical frame structures. Under the same pilot cost, compared with carrier synchronization schemes using classical frame structures, carrier synchronization schemes using optimized structure 1 and optimized structure 2 have achieved significant performance gains. Taking $\text{BER}=10^{-4}$ as an example, the performance gains brought by these two optimized structures are greater than 2.5dB and greater than 2dB, respectively. This algorithm, like the Gardner algorithm, only requires twice the symbol rate sampling, but unlike the Gardner algorithm, which directly uses the received data for bias estimation, it fully utilizes the excellent correlation characteristics of the gray sequence. The received data is first cross correlated with the local gray sequence, and then the sampling timing deviation is estimated based on the correlation peak.

This algorithm greatly reduces the interference of noise on estimated values and improves estimation accuracy. Considering the complexity of FPGA implementation in the project, this article proposes specific hardware implementation methods such as combining error estimation with ROM lookup tables. Since only the first pilot block is used for the coarse estimation of the first step frequency offset, the length of the first pilot block can be increased to improve the estimation accuracy of the first step frequency offset estimation algorithm while the pilot cost remains unchanged. The optimized frame structure obtained from Scheme 1 is referred to as optimization structure -1 in the following text. Compared with non-Polynomial interpolation filters with high implementation complexity, polynomial interpolation filters with simple structure can also achieve excellent performance. Reference analyzes the performance of several commonly used interpolation filters in sampling timing synchronization in detail and points out that linear interpolation filters have excellent performance, simple structure, and can be applied to most occasions. Considering the actual situation of the project, this paper uses Linear interpolation filter to correct sampling timing deviation.

3. CONCLUSION

This paper proposes an effective carrier synchronization scheme for low orbit satellite communication systems based on SCMA technology to address the problem of large Doppler frequency shift. Firstly, coarse estimation of frequency offset is used to capture and compensate for large Doppler frequency shift; Then, the remaining frequency offset is captured and fine compensated using fine estimation of frequency offset; Finally, the maximum likelihood algorithm is used to estimate the residual frequency offset and phase offset. Based on existing sampling timing synchronization algorithms, a sampling timing synchronization algorithm suitable for SSB single carrier frame structure was studied. The traditional SSB sampling timing synchronization algorithm was combined with the specific situation of this project, and the sampling timing synchronization algorithm based on gray sequence cross correlation operation was analyzed. Simulation verification was conducted, and the feasible conclusion of the algorithm was drawn. Finally, the algorithm was applied to the hardware implementation of the project and FPGA design verification was carried out, successfully resolved the impact of sampling timing deviation on the baseband receiver of the project.

4. REFERENCES

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