

# Design and Implementation of a Multi-Function Test Instrument Based on FPGA

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**Abstract:** With the continuous development of electronic testing technology, the limitations of traditional measurement instruments in terms of portability, integration, and flexibility are becoming increasingly apparent. To meet the demand for multifunctional, high-performance portable instruments in scientific research, education, and engineering fields, this paper proposes an integrated testing system based on FPGA—"Intelligent Measurement Wizard". The system innovatively integrates function modules such as signal generator, oscilloscope, and logic analyzer on a single platform, utilizing Ethernet communication to achieve high-speed data transmission while supporting real-time parameter adjustment and multi-board cascade expansion. Through the application of RISC-V soft-core transplantation and DDR3 storage technology, the system achieves 99% frequency accuracy, 15-35MSPS sampling rate, and 4-channel logic analysis capability while maintaining portability. This paper will discuss the system architecture, module design, performance testing, and other aspects, providing new solutions for the development of portable testing instruments.

**Keywords:** FPGA Platform; RISC-V Soft-core Transplantation; Oscilloscope; Signal Generator; Logic Analyzer

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## 1. Introduction

With the advancement of electronic testing technology towards integration and portability, traditional instruments (e.g., oscilloscopes, signal generators) face limitations due to their isolated functionality and poor interoperability[1]. To address this, we developed an FPGA-based "Intelligent Measurement Wizard" system that innovatively integrates signal generation, waveform acquisition, logic analysis, and spectral processing into a single device. The system enables high-speed data interaction with host software via Ethernet, incorporates a RISC-V soft core for enhanced flexibility[2], and supports multi-board expansion through UART cascading.

## 2. Main technical features

The system employs a highly integrated design that incorporates multiple functional modules including signal generators, oscilloscopes, and logic analyzers into a unified hardware platform, accompanied by the development of host software with an intuitive interface that supports flexible configuration and real-time adjustment of system parameters[4]. The oscilloscope module innovatively integrates FFT spectrum analysis capabilities while maintaining traditional time-domain waveform display functions, enabling users to perform frequency-domain characteristic analysis on acquired signals through the host software. The logic analyzer module adopts a combined design of ping-pong buffering mechanism and DDR3 storage technology, achieving high-speed continuous acquisition of multi-channel signals and massive data storage[5]. The system ensures high-speed data interaction with the host computer through Gigabit Ethernet communication protocol, while supporting multi-level hardware expansion via inter-board UART communication, theoretically allowing flexible cascading and functional combination of N boards[6]. Notably, the transplantation of a RISC-V soft core processor into the FPGA architecture significantly enhances the system's real-time processing capabilities and overall architectural scalability.

## 3. Key Performance Indicators

### 3.1 Signal Generator Performance

**Frequency Range & Accuracy:** The output frequency covers a full range from 1 Hz to 16 MHz, with a minimum step resolution of 1 Hz. The fundamental frequency accuracy across the entire range is better than 99%.

**Amplitude Characteristics:** The output voltage peak-to-peak accuracy is high, reaching 99.8% in the 1 Hz - 3 MHz range (0-5V); 95% in the 3 MHz - 10 MHz range (maximum amplitude decays with frequency, 1V max @10MHz); and 84% in the 10 MHz - 16 MHz range (0.4V max @16MHz). The amplitude adjustment resolution is 0.1 V.

**Waveform Types:** Supports the output of four standard waveforms: Sine, Square, Triangle, and Sawtooth.

### 3.2 Oscilloscope Performance

**Sampling Capability:** Provides four adjustable sampling rate grades: 15 MS/s, 20 MS/s, 25 MS/s, and 35 MS/s, meeting the acquisition needs for signals of different bandwidths.

**Display & Measurement:** Features 4 adjustable levels of vertical display resolution for observing waveform details. Integrated FFT spectrum analysis function boasts a frequency analysis accuracy of 99% within the 0 - 100 kHz range and 95% at frequencies above 1 MHz, with stable voltage measurement accuracy across the entire frequency band.

### 3.3 Logic Analyzer

**Acquisition Capability:** Supports parallel acquisition of 4 channels of digital signals, with a maximum sampling rate of 50 MS/s (optional grades: 5M, 10M, 25M, 50M).

**Triggering & Storage:** Features flexible trigger settings, supporting rising edge, falling edge, and arbitrary level triggering on any channel. Utilizes large-capacity DDR3 cache, with a maximum storage depth of 1024 MByte, ensuring long-term, uninterrupted data acquisition.

**TransferPerformance:** Optimizes the Ethernet communication protocol to achieve a high data transfer rate of 7.79 ns/byte, guaranteeing the real-time upload of massive data sets.

#### 4. Main Innovations

**Highly Integrated Design:** Integrates four major functions (signal generator, oscilloscope, logic analyzer, and FFT) into a single FPGA platform, significantly enhancing portability and cost-effectiveness.

**High-Speed Data Pipeline:** Employs an innovative "ping-pong buffering" mechanism with dual DDR3 memory. Enables uninterrupted data acquisition with 7.79 ns/byte transfer rate.

**Reconfigurable Processing Platform:** Integrates RISC-V soft core into FPGA, combining hardware processing speed with software programming flexibility for future functional evolution.

### 5. System Composition and Functional Description

#### 5.1 Overall Introduction

The system adopts a design philosophy of hardware architecture based on FPGA working in coordination with host computer software, constructing a highly integrated multi-functional test platform. Its core is to enable interactive uplink and downlink data communication through Ethernet, with various functional modules processing in parallel within the FPGA, achieving integrated operations of signal generation, acquisition, and analysis. The overall hardware and functional architecture of the system is shown in Figure 1, which clearly illustrates the data flow and control relationships between the core modules:

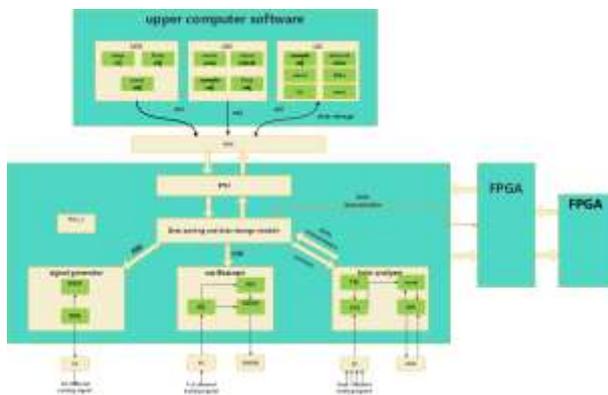


Figure. 1 Overall block diagram

#### 5.2 Ethernet Communication Module

As the core interface for system-host computer interaction, the Ethernet module adopts a layered architecture design to ensure reliable and efficient data communication. It consists of PLL clock management unit, RGMII/GMII protocol conversion unit, UDP data transceiver unit, CRC checksum unit, and receive FIFO buffer.

The PLL unit compensates for clock-data skew caused by PCB trace delays through phase offset compensation technology. The RGMII-to-GMII protocol conversion unit enables protocol adaptation between physical and data link layers. The UDP\_RX unit performs target MAC/IP address verification, packet parsing, and 8-bit to 32-bit data width conversion, while the UDP\_TX unit handles Ethernet packet

encapsulation and transmission. The CRC unit ensures data integrity, and REC\_FIFO serves as a data buffer to resolve cross-clock domain data processing issues.

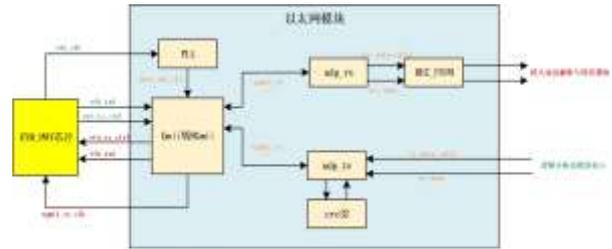


Figure. 2 Ethernet module block diagram

#### 5.3 Data Parsing and Forwarding Module

This module performs the core functions of system instruction parsing and data routing, employing a dual-mode working mechanism.

When receiving Ethernet data, the module parses the packet content according to the communication protocol shown in Table 1 and forwards valid instructions to cascaded boards via UART. In the absence of Ethernet data, it directly transparently transmits UART data. This design enables seamless collaboration and instruction synchronization among multiple boards.

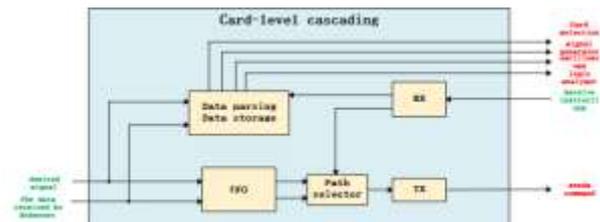


Figure. 3 Data Parsing Module Block Diagram

#### 5.4 Signal Generator Module

Built on Direct Digital Synthesis (DDS) technology, it comprises four core subsystems: phase accumulator, phase modulator, waveform data table ROM, and D/A converter.

Through the introduction of frequency/amplitude adjustment algorithms and DC offset correction technology, it achieves precise generation of four waveforms (sine, square, triangle, sawtooth) within the 1Hz-16MHz frequency range while maintaining reference voltage stability. All parameters can be adjusted in real-time through the host computer.

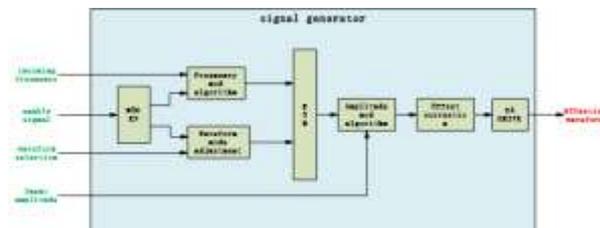


Figure. 4 Block diagram of the signal generator module

#### 5.5 Oscilloscope Module

Utilizes a multi-stage pipeline architecture containing three subsystems: signal acquisition, data processing, and display driver.

The input unit employs programmable PLL clock technology, supporting four sampling rate adjustments from 15-35MSps.

The processing unit implements time/frequency domain analysis functions through a dual-mode FFT processor, using RAM mapping technology to correlate sampling data with screen coordinates in real-time. The output unit initializes the HDMI controller via I<sup>2</sup>C protocol, establishes 1920×1080@60Hz DE driving timing, and achieves synchronous display of waveforms and background grids.

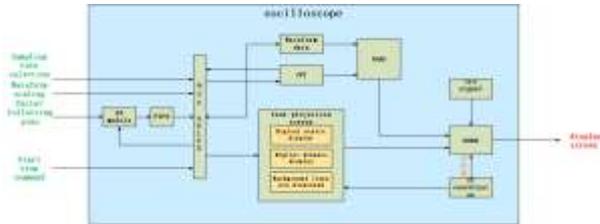


Figure. 5 Oscilloscope module block diagram

### 5.6 Logic Analyzer Module

Employs a multi-stage pipeline architecture to achieve high-speed acquisition and analysis of 4-channel digital signals.

The clock divider module generates configurable sampling clocks; the trigger module integrates edge detection algorithms supporting rising/falling/arbitrary edge trigger modes[7]; the acquisition module uses 8-bit shift register arrays for 4-channel parallel signal acquisition; the ping-pong buffer architecture combined with AXI bus protocol enables high-speed DDR3 read/write operations, ultimately achieving a data transfer rate of 7.79ns/byte through Gigabit Ethernet[8].

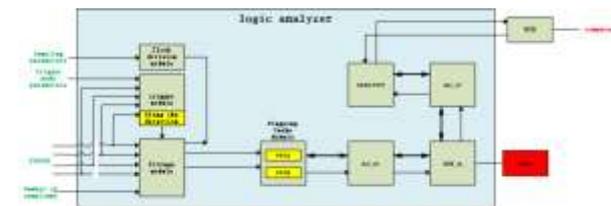


Figure. 6 logic analyzer module block diagram

## 6. System Implementation and Debugging

### 6.1 Physical Platform

This study presents the "Intelligent Measurement Wizard," a dual-FPGA platform leveraging two PanGu 50H development boards in a master-slave cascade architecture. Precision hardware design ensures stable high-speed signal transmission, while a Gigabit Ethernet interface enables real-time data exchange at 7.79 ns/byte—sufficient for multi-channel requirements. The system's innovative serial communication protocol facilitates synchronous multi-board coordination, significantly expanding scalability and channel capacity.



Figure. 7 System physical diagram

### 6.2 Signal Generator verification

The signal generator module employs a 14-bit high-precision DAC for waveform output. Test results show: output accuracy reaches 99.8% (0-5V) in the 1Hz-3MHz range, and maintains

95% accuracy in the 3MHz-10MHz range (1V max @10MHz). As shown in Figures 8 and 9, the system can generate stable sine and square wave signals.

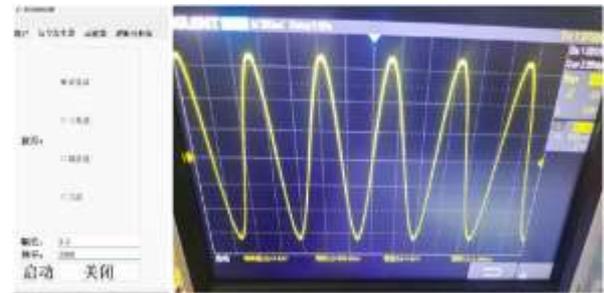


Figure. 8 Sine wave signal diagram

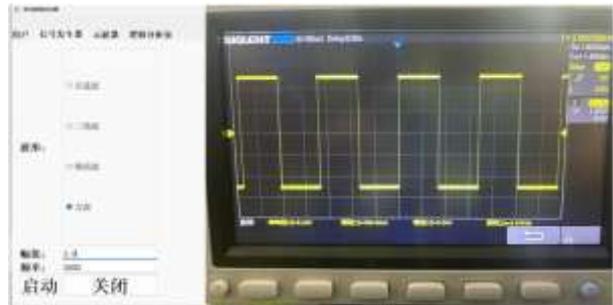


Figure. 9 Square wave signal diagram

### 6.3 Oscilloscope Module Test Results

The oscilloscope module supports a maximum sampling rate of 35MSps with 4 adjustable levels of vertical resolution. As shown in Figure 10, the system successfully implements waveform zooming function, enabling clear capture of signal details. The FFT spectrum analysis function achieves 99% frequency accuracy within the 0-100kHz range and maintains 95% accuracy above 1MHz. Figure 10 demonstrates the spectral analysis results of a 5.1V/100kHz sine wave.



Figure. 10 Oscilloscope function test diagram

### 6.4 Logic Analyzer Verification

The logic analyzer module implements 4-channel parallel acquisition with a maximum sampling rate of 50MSps. Using a "ping-pong buffering" mechanism and dual-DDR3 architecture, it achieves a storage depth of 1024MB. As shown in Figure 11, the system successfully captures and parses 8'h12 (00010010) serial data, verifying trigger functionality and data parsing capability. Transmission performance was verified by Wireshark software: transmission of 51200 bytes of data requires only 399μs (Figure 11), with a measured transmission rate of 7.79ns/byte, meeting high-speed data acquisition requirements.

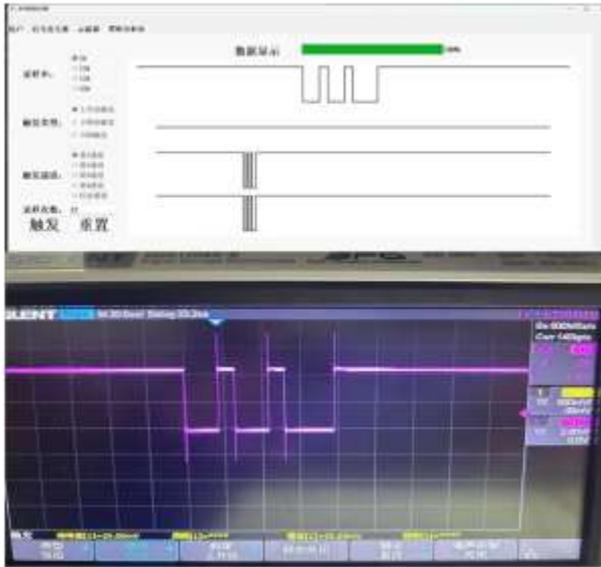


Figure. 11 Logic Analyzer function test diagram

## 7. Conclusion

This research successfully developed an FPGA-based "Intelligent Measurement Wizard" multi-function test system, achieving highly integrated design of signal generator, oscilloscope and logic analyzer. The system adopts RISC-V soft-core architecture to enhance processing flexibility, realizes 7.79ns/byte high-speed data transmission through Ethernet interface, and innovatively supports multi-board cascade expansion. Performance tests demonstrate: signal generator achieves 1Hz-16MHz frequency range (accuracy > 99%), oscilloscope supports 35MSps sampling with FFT analysis, and logic analyzer implements 4-channel 50MSps acquisition with 1024MB storage depth. The system innovatively employs ping-pong buffering combined with DDR3 architecture to ensure real-time data acquisition, with supporting host software providing comprehensive parameter control and data visualization functions. Experimental verification shows that the system excels in measurement accuracy, transmission rate and functional integration,

providing an innovative solution for the development of portable test instruments with significant engineering application value.

## 8. References

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