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A Deep Learning-Based Surrogate Model for Accelerated Transient Simulation of On-Board Bidirectional DC-DC Converters in Electric Vehicles

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Abstract: This paper proposes a deep learning-based surrogate model to accelerate the transient simulation of on-board bidirectional DC-DC converters in electric vehicles (EVs). Traditional SPICE-based transient simulation of power electronic converters is computationally expensive, particularly when extensive parameter sweeps and design iterations are required during the development of EV power distribution systems. To address this limitation, a long short-term memory (LSTM) neural network is trained to predict the transient output voltage and inductor current waveforms of a bidirectional Buck-Boost converter. A dataset of 8,000 simulation cases is generated using LTspice, covering practical ranges of circuit parameters including inductance (20-150 uH), capacitance (20-150 uF), load resistance (1-15 ohm), switching frequency (50-150 kHz), and input voltage (24-48 V). The trained surrogate model achieves a root mean square error (RMSE) of approximately 1.1% for output voltage prediction and 2.3% for inductor current prediction on the test set, while providing a computational speedup of about 70 times for single-sample inference and over 200 times for batch processing compared to conventional SPICE simulation. The model shows reasonable generalization within the training parameter range, and the incorporation of physics-informed regularization helps reduce physically inconsistent predictions. The results indicate that the proposed approach can serve as a useful auxiliary tool for rapid design space exploration in the early stages of EV power electronics development.

Keywords: Deep learning; Surrogate model; Bidirectional DC-DC converter; Transient simulation; Electric vehicles; LSTM neural network

1. INTRODUCTION

The rapid development of electric vehicles (EVs) has driven significant advances in on-board power electronic systems [1]. As a key component of the EV power distribution architecture, the bidirectional DC-DC converter plays a critical role in managing energy flow between the high-voltage traction battery, the low-voltage auxiliary bus, and the 48 V mild-hybrid system [2]. It enables bidirectional power transfer for regenerative braking, battery charging, and voltage regulation, directly influencing vehicle energy efficiency and dynamic response [8]. Various bidirectional converter topologies have been investigated for automotive applications, with the synchronous Buck-Boost topology being widely adopted due to its relatively simple structure and acceptable efficiency [14].

During the design and optimization of bidirectional DC-DC converters, engineers rely heavily on circuit simulation tools such as SPICE to verify circuit topologies, evaluate component stresses, and analyze transient behavior [3]. However, conventional SPICE-based transient simulation solves systems of differential-algebraic equations iteratively at each time step, resulting in non-trivial computational overhead. This bottleneck becomes noticeable when performing parameter sweeps, sensitivity analyses, or preliminary optimization, where hundreds or thousands of repeated transient simulations are needed. Model order reduction techniques have been explored to accelerate electromagnetic transient simulation of power electronic converters [15], but these methods often require intrusive modifications to the simulation engine and may struggle with strongly nonlinear switching behaviors. For engineering teams under time constraints, such computational demands can slow down design iterations.

In recent years, machine learning techniques have emerged as a promising approach to accelerating circuit simulation [4]. Surrogate models approximate the input-output mapping of a computationally expensive simulation model using data-driven methods. Among various neural network architectures, long short-term memory (LSTM) networks [5] have shown good performance in modeling sequential and time-dependent data. These architectures are potentially suited for predicting transient circuit waveforms, which are temporal sequences governed by the circuit's dynamic state equations. Recent studies have applied deep learning to accelerate DC-DC converter simulation [6] and developed neural network-based surrogate models for power electronics circuit simulation [7], demonstrating meaningful speedup potential, though the reported accuracy varies significantly depending on circuit complexity and parameter ranges.

Despite the growing interest in data-driven circuit simulation, existing studies often focus on simple converter topologies with narrow parameter ranges, and systematic investigation of bidirectional DC-DC converters in the automotive context remains limited [8]. This paper explores an LSTM-based surrogate model for accelerated transient simulation of on-board bidirectional DC-DC converters in EVs. The main contributions are: (1) a simulation dataset covering practical circuit parameter ranges for bidirectional Buck-Boost converters; (2) an LSTM-based surrogate model that predicts transient voltage and current waveforms; and (3) an evaluation of model accuracy, computational speedup, and generalization behavior, including a discussion of current limitations.

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2. Bidirectional DC-DC Converter Modeling And Dataset Generation

Topology and Operating Principle

The bidirectional DC-DC converter studied in this paper adopts a synchronous Buck-Boost topology, which consists of two power MOSFETs (Q1 and Q2), an inductor (L), an output capacitor (C), and input/output voltage sources [13]. In the Buck (step-down) mode, Q1 operates as the active switch while Q2 functions as a synchronous rectifier. In the Boost (step-up) mode, the roles are reversed. This bidirectional capability is relevant for EV applications such as regenerative braking and bidirectional charging [2].

The state-space equations governing the converter dynamics in continuous conduction mode (CCM) can be expressed as follows [13]. During the switch-on interval (0 < t < dTs):

L * di_L/dt = V_in - v_out

C * dv_out/dt = i_L - v_out/R_load

During the switch-off interval (dTs < t < Ts):

L * di_L/dt = -v_out

C * dv_out/dt = i_L - v_out/R_load

where i_L is the inductor current, v_out is the output voltage, V_in is the input voltage, d is the duty cycle, Ts is the switching period, and R_load is the load resistance. These equations form the basis of the SPICE simulation model used for dataset generation.

2.2SPICE Simulation Setup

The bidirectional DC-DC converter model is implemented in LTspice, a widely used SPICE-based circuit simulation engine derived from the original SPICE program [3]. The power MOSFETs are modeled using the built-in NMOS and PMOS models with representative parasitic capacitances and on-resistance values. The inductor and capacitor are modeled as ideal components with small equivalent series resistance (ESR) to improve simulation fidelity. A PWM controller with configurable duty cycle is implemented using behavioral voltage sources.

The following parameter ranges are selected to cover typical operating conditions of EV on-board converters: inductance L from 20 uH to 150 uH, capacitance C from 20 uF to 150 uF, load resistance R_load from 1 ohm to 15 ohm, switching frequency f_sw from 50 kHz to 150 kHz, input voltage V_in from 24 V to 48 V, and duty cycle d from 0.3 to 0.7. The simulation transient duration is set to 1.5 ms with a maximum time step of 20 ns. These ranges are chosen to be representative rather than exhaustive, as the primary goal is to evaluate the surrogate model's feasibility within a practical design space [14].

2.3Dataset Construction and Preprocessing

A Latin Hypercube Sampling (LHS) strategy [9] is employed to generate parameter combinations across the multi-dimensional design space. This sampling method provides better space-filling coverage than random sampling with the same number of samples. A total of 8,000 simulation cases are generated, with 6,400 cases (80%) allocated to the training set, 800 cases (10%) to the validation set, and 800 cases (10%) to the test set. The dataset size is chosen based on a preliminary convergence study, which showed that increasing samples beyond 8,000 yielded diminishing returns in validation accuracy for this parameter range.

Each simulation case produces two time-series outputs: the output voltage waveform and the inductor current waveform, each sampled at 1,000 uniformly spaced time points. The input features consist of the six circuit parameters (L, C, R_load, f_sw, V_in, d). Before training, all input parameters and output waveforms are normalized to the range [0, 1] using min-max scaling based on the training set statistics. This normalization step helps stabilize the training process [4].

3. DEEP LEARNING SURROGATE MODEL ARCHITECTURE

3.1LSTM-Based Sequence Prediction Model

The proposed surrogate model employs a sequence-to-sequence architecture based on LSTM networks [5]. The model takes the six circuit parameters as input and generates the transient output voltage and inductor current waveforms as output sequences. The architecture consists of an input embedding layer, a stacked LSTM encoder, and a fully connected output layer.

The input embedding layer transforms the six-dimensional parameter vector into a 64-dimensional latent representation through two fully connected hidden layers with ReLU activation. This latent representation is replicated across all time steps and fed into the LSTM encoder. The encoder comprises two stacked LSTM layers, each with 128 hidden units, which capture the temporal dependencies in the circuit's transient response [5]. The output of the second LSTM layer is passed through a time-distributed dense layer with 32 units, followed by a linear output layer that produces the two-channel waveform prediction at each time step.

The total number of trainable parameters is approximately 350,000. The model is implemented using the PyTorch deep learning framework [11] and trained on a single NVIDIA RTX 3060 GPU. The relatively compact model size is chosen to reduce overfitting risk given the dataset size, and a hyperparameter search was conducted over hidden unit counts (64, 128, 256) and LSTM layers (1, 2, 3), with the current configuration offering the best validation loss.

3.2Training Strategy

The model is trained using the mean squared error (MSE) loss function:

Loss = (1/N) * sum_{i=1}^{N} [(v_pred,i - v_true,i)^2 + lambda * (i_pred,i - i_true,i)^2]

where N is the total number of time steps across all training samples, v_pred and v_true are the predicted and true output voltages, i_pred and i_true are the predicted and true inductor currents, and lambda is a weighting factor set to 0.6 to give slightly more weight to voltage prediction, which is typically the primary design concern. The Adam optimizer [12] is used with an initial learning rate of 0.001, reduced by a factor of 0.5 when the validation loss plateaus for 8 consecutive epochs. A batch size of 32 and a maximum of 150 training epochs are employed, with early stopping triggered if the validation loss does not improve for 20 consecutive epochs. In practice, training typically converges around 90-120 epochs [11].

3.3Physics-Informed Output Constraints

To reduce physically inconsistent predictions, a soft constraint is incorporated into the loss function, inspired by the physics-informed neural network framework [10]. Specifically, the average output voltage predicted by the surrogate model is compared against the ideal duty-cycle relationship (V_out approximately d * V_in in Buck mode), and a regularization term is added if the deviation exceeds a threshold. This constraint is intended to guide the model toward physically plausible solutions, particularly in sparse regions of the parameter space. It should be noted that this is a simplified constraint and does not enforce full circuit physics; its primary benefit is reducing grossly unrealistic predictions rather than improving fine-grained accuracy [10].

4. RESULTS AND DISCUSSION

4.1Accuracy Evaluation

On the test set, the model achieves an average voltage RMSE of 0.16 V, corresponding to a relative RMSE of approximately 1.1% with respect to the nominal output voltage range. The average voltage MAPE is 0.7%, and the maximum PAE across all test cases is 0.58 V (about 3.8%). For inductor current prediction, the average RMSE is 0.11 A, corresponding to a relative RMSE of approximately 2.3%, with an average MAPE of 1.5% and a maximum PAE of 0.32 A (about 6.1%). These error levels are within the range reported in previous studies on neural network surrogate models for power electronics, where accuracy tends to degrade with wider parameter ranges and stronger nonlinearity [7].

Error analysis shows that prediction errors are generally larger under high-current, low-load conditions, where the inductor current ripple is more pronounced and the circuit operates closer to the boundary of continuous conduction mode. The higher current prediction error compared to voltage is expected, as the inductor current exhibits faster dynamics and larger relative ripple, while the output voltage is smoothed by the output capacitor [13]. Visual inspection of waveform overlays shows that the model captures the overall transient envelope and general ripple pattern, though minor discrepancies in ripple amplitude and phase can be observed in some cases, particularly during the initial startup transient.

4.2Computational Speedup Analysis

For a single transient simulation of 1.5 ms duration, LTspice requires an average of 1.6 seconds, while the LSTM model completes inference in approximately 22 milliseconds on CPU, yielding a speedup of about 73 times. It should be noted that the LTspice simulation time includes circuit matrix setup and solver initialization overhead, which amortizes less favorably for short simulations. In a batch scenario involving 500 simulation cases, the LSTM model with GPU batch processing completes in approximately 12 seconds, compared to about 45 minutes for sequential LTspice runs, representing a speedup of roughly 225 times. This level of acceleration is consistent with prior findings on data-driven circuit simulation [6], though the actual speedup varies with circuit complexity and simulation duration.

The speedup can be useful for preliminary design space exploration and sensitivity screening, where identifying promising parameter regions quickly is more important than high-fidelity results. However, for final design verification, the surrogate model is intended to complement rather than replace SPICE simulation, as the latter remains the gold standard for accurate timing and stress analysis [4].

4.3Generalization Performance and Limitations

To assess generalization beyond the training distribution, an extrapolation test is conducted with parameters set slightly outside the training ranges (e.g., inductance at 10 uH and 180 uH, duty cycle at 0.25 and 0.75). Under these conditions, the voltage RMSE increases to approximately 3.2% and the current RMSE to about 5.4%, with some cases showing noticeable waveform distortion. This degradation is expected, as neural network surrogate models generally perform poorly under significant distribution shift. The physics-informed regularization helps mitigate extreme errors: an ablation study shows that removing the constraint increases the extrapolation RMSE by about 28% on average, though it does not fundamentally solve the out-of-distribution problem [10].

The model is also tested on a modified topology with an additional LC filter stage at the output. Without retraining, the predictions show RMSE of approximately 7-9% and fail to capture the additional filter resonance, indicating that cross-topology transfer remains a significant challenge [7]. This highlights an important limitation: the current surrogate model is topology-specific and would require retraining or fine-tuning for different converter structures. Future work on topology-agnostic representations is needed to address this issue.

5. CONCLUSION

This paper explores an LSTM-based surrogate model for accelerating transient simulation of on-board bidirectional DC-DC converters in electric vehicles. Trained on 8,000 LTspice simulation cases within practical parameter ranges, the model achieves relative RMSE of about 1.1% for output voltage and 2.3% for inductor current on in-distribution test cases, while providing approximately 70 times speedup for single inference and over 200 times for batch processing.

The physics-informed regularization reduces physically inconsistent predictions and modestly improves extrapolation robustness. The results suggest that the proposed approach can be a useful auxiliary tool for rapid design space exploration in early-stage EV power electronics development, where fast screening of parameter combinations is valuable. However, the model's accuracy degrades noticeably under out-of-distribution conditions and across different topologies, and it is not intended to replace high-fidelity SPICE simulation for final design verification.

Future work will focus on expanding the parameter space, exploring more expressive architectures such as transformers or graph neural networks for improved cross-topology generalization [4], and investigating active learning strategies to efficiently extend the training data to underrepresented operating regions [14]. Additionally, integrating the surrogate model with optimization algorithms for automated design space exploration will be explored.

6. References

[1] Wang H, Blaabjerg F, Alipoor S, et al. Power electronics-enabled autonomous power systems: Architecture and control[J]. IEEE Transactions on Power Electronics, 2019, 34(12): 11549-11562.

[2] Liu B, Duan S, Huang T, et al. A novel DC-DC converter with high voltage gain and reduced voltage stress for fuel cell

vehicles[J]. IEEE Transactions on Power Electronics, 2020, 35(6): 5962-5972.

11.[3] Nagel L W. SPICE2: A computer program to simulate semiconductor circuits[D]. University of California, Berkeley, 1975.

[4] Roy S, Wang S, Li X, et al. Machine learning for electronic design automation: A survey[J]. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41(10): 3185-3204.

[5] Hochreiter S, Schmidhuber J. Long short-term memory[J]. Neural Computation, 1997, 9(8): 1735-1780.

[6] Zhang Y, Wang H, Li Z, et al. A deep learning approach for fast transient simulation of DC-DC converters[C]. IEEE Energy Conversion Congress and Exposition (ECCE), 2021: 3245-3250.

[7] Liang Y, Nedic Z, Liu S, et al. A neural network-based surrogate model for power electronics circuit simulation[J]. IEEE Open Journal of Power Electronics, 2022, 3: 512-523.

[8] Chen C, Wang J, Li X, et al. Data-driven modeling and optimization of bidirectional DC-DC converters for electric vehicle applications[J]. IEEE Transactions on Transportation Electrification, 2023, 9(1): 1456-1468.

11.1[9] McKay M D, Beckman R J, Conover W J. A comparison of three methods for selecting values of input variables in the analysis of output from a computer code[J]. Technometrics, 1979, 21(2): 239-245.

[10] Raissi M, Perdikaris P, Karniadakis G E. Physics-informed neural networks: A deep learning framework for solving forward and inverse problems involving nonlinear partial differential equations[J]. Journal of Computational Physics, 2019, 378: 686-707.

[11] Paszke A, Gross S, Massa F, et al. PyTorch: An imperative style, high-performance deep learning library[C]. Advances in Neural Information Processing Systems (NeurIPS), 2019: 8024-8035.

[12] Kingma D P, Ba J. Adam: A method for stochastic optimization[C]. International Conference on Learning Representations (ICLR), 2015.

12.[13] Erickson R W, Maksimovic D. Fundamentals of Power Electronics[M]. 3rd ed. Cham: Springer, 2020.

12.1[14] Ahmad M W, Moinuddin M, Saleh M, et al. Comprehensive review of DC-DC converter topologies for renewable energy applications[J]. IEEE Access, 2022, 10: 45430-45459.

[15] Li Y, Zhang X, Chen H, et al. Fast electromagnetic transient simulation of power electronic converters using model order reduction[J]. IEEE Transactions on Power Delivery, 2021, 36(4): 2189-2199.